



**PATENT APPLICATION**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of

Yoichi YAMADA

Group Art Unit: 2187

Application No.: 09/720,142

Examiner: B. Peugh

Filed: December 21, 2000

Docket No.: 107300

For: SEMICONDUCTOR INTEGRATED CIRCUIT

**AFFIDAVIT**

**RECEIVED**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

JAN 16 2004

Technology Center 2100

Sir:

I Yoichi Yamada do hereby aver that I am not aware of  
any instance of the art described in the above-referenced patent application as "conventional"  
that qualifies as statutory prior art in the United States under 35 U.S.C. §102.

Respectfully submitted,

Yoichi Yamada

Date: January 13, 2004